FACULTY OF ELECTRICAL ENGINEERING

SUBJECT CARD

Name in Polish:	**Układy logiczne**
Name in English:	**Logic design**
Main field of study (if applicable):	**Electrical Engineering**
Specialization (if applicable):	**Electrical Power Engineering**
Level and form of studies:	**2nd level, full-time**
Kind of subject:	**optional**
Subject code:	**ELR052114**
Group of courses:	**NO**

	Lecture	Classes	Laboratory	Project	Seminar
Number of hours of organized classes in University (ZZU):	30		15		
Number of hours of total student workload (CNPS):	60		30		
Form of crediting:	examination		crediting with grade		
For group of courses mark (X) final course:					
Number of ECTS points:	2		1		
including number of ECTS points for practical (P) classes :			1		
including number of ECTS points for direct teacher-student contact (BK) classes:	1.40		0.70		

PREREQUISITES RELATING TO KNOWLEDGE, SKILLS AND OTHER COMPETENCES

1. Knowledge of basic digital circuits.
2. Knowledge of the practical implementation and verification of simple digital circuits.

SUBJECT OBJECTIVES

C1. Knowledge of the most popular medium-scale digital systems integration, such as: adders, comparators, counters, registers, multiplexers, demultiplexers, code converters.

C2. Acquisition of theoretical and practical knowledge of combinational logic circuits: canonical form, Karnaugh map, the Quine–McCluskey algorithm, the hazard phenomenon.

C3. Acquisition of theoretical and practical knowledge of sequential asynchronous logic circuits: the method of consecutive switching tables, Moore and Mealy type automata , the race phenomenon.

C4. Acquisition of theoretical and practical knowledge of sequential synchronous logic circuits.

C5. Familiarization with methods concerning: presenting a logic circuit operation, selecting of design methods, practical analysis/synthesis methods and ways of implementing logic circuits. Ability of practical team working.

SUBJECT LEARNING OUTCOMES

relating to knowledge:

PEU_W01	Student has a knowledge of the architecture and operating the most popular medium-scale digital systems integration.
PEU_W02	Student has a knowledge of operating and analysis/synthesis methods of combinational logic circuits.
PEU_W03	Student has a knowledge of operating and analysis/synthesis methods of sequential (synchronous and asynchronous) logic circuits.

relating to skills:

PEU_U01	Student has the ability of practical use the most popular medium-scale digital systems integration.
PEU_U02	Student is able to conduct both analysis and synthesis, as well as to implement combinational logic circuits with use the optimization methods, with eliminating a hazard phenomenon.
PEU_U03	Student is able to conduct both analysis and synthesis, as well as to implement asynchronous (with eliminating of race phenomenon) and synchronous logic circuits with use the optimization methods.

relating to social competences:

PEU_K01	Student can competently act alone and cooperate in the team that develops a complex engineering project.

PROGRAMME CONTENT		
Form of classes - lecture		**Number of hours:**
Lec 1	Introduction. Establishing of conditions for passing the course. Basics of Boole algebra. Typical logic gates and circuits and their graphic symbols.	2
Lec 2	Canonical forms of switching function, the principles of minimization.	2
Lec 3	Design of combinational logic circuits - the Karnaugh maps method. Eliminating a hazard phenomenon.	2
Lec 4	Design of combinational logic circuits with Quine–McCluskey algorithm (binary and decimal version) and with use of the multiplexer.	2
Lec 5	Design of combinational logic circuits with Quine–McCluskey algorithm (binary and decimal version) and with use of the multiplexer. (continued)	2
Lec 6	The minimizing of ill-defined functions.	2
Lec 7	The minimizing of multi-output functions.	2
Lec 8	Sequential automata – types, general characteristic, memory implementation methods. The rules of sequential automata design with use of the method of consecutive switching tables.	2
Lec 9	The examples of sequential automata design with use of the method of consecutive switching tables, with the problem of infeasibility switching table.	2
Lec 10	Sequential automata – description of Moore and Mealy type automata, time diagrams, switching and output tables, graphs. The rules of sequential asynchronous automata design with use of the method of switching and output tables.	2
Lec 11	The examples of sequential asynchronous automata design with use of the method of switching and output tables. Eliminating of race phenomenon.	2
Lec 12	Sequential synchronous automata design.	2
Lec 13	Typical switching circuits, principles of design and testing using simulation programmes and educational models.	2
Lec 14	Asynchronous and synchronous counters. Principles of design modulo ≠ 2^n binary counters.	2
Lec 15	Shift registers. Principles of operation and design. Code converters. Principles of operation and design.	2
	Total hours:	**30**

Form of classes - laboratory		**Number of hours:**
Lab 1	Presentation of the Rules of Procedure Health and Safety Laboratory. Establish rules for passing. General knowledge of the laboratory stand: educational models, simulation programme.	1
Lab 2	Sequential asynchronous automata design with use of the method of switching and output tables. Implementation with use of gates.	2
Lab 3	Sequential asynchronous automata design with use of the method of switching and output tables. Implementation with use of gates. (continued)	2
Lab 4	Sequential asynchronous automata design with use of the method of switching and output tables. Implementation with use of flip-flops.	2
Lab 5	Sequential asynchronous automata design with use of the method of consecutive switching tables.	2
Lab 6	Multiplexers, demultiplexers, code converters.	2
Lab 7	Sequential synchronous automata design.	2
Lab 8	Adders, comparators, counters, registers.	2
	Total hours:	**15**

TEACHING TOOLS USED
N1. Informative lecture.
N2. Educational models of digital circuits.
N3. Programme for simulating digital circuits.
N4. Project report.

EVALUATION OF SUBJECT LEARNING OUTCOMES ACHIEVEMENT		
Evaluation *F – forming (during semester)* *P – concluding (at semester end)*	**Educational effect number**	**Way of evaluating educational effect achievement**
F1(W)	PEU_W01 PEU_W02 PEU_W03	attendance on classes
F2(W)	PEU_W01 PEU_W02 PEU_W03	final exam
P(W)	P = 0,1F1 + 0,9F2	
F1(L)	PEU_U01 PEU_U02 PEU_U03	activity
F2(L)	PEU_U01 PEU_U02 PEU_U03 PEU_K01	laboratory report
P(L)	P = 0,3 F1 + 0,7F2	

PRIMARY AND SECONDARY LITERATURE

PRIMARY LITERATURE:

[1] Układy logiczne. Ćwiczenia laboratoryjne. Skrypt Politechniki Wrocławskiej pod red. Mirosława Łukowicza. Oficyna Wydawnicza Politechniki Wrocławskiej, Wrocław 2002

SECONDARY LITERATURE:

[1] Wilkinson B., Układy cyfrowe. WKŁ, Warszawa, 2000
[2] Skorupski A., Podstawy techniki cyfrowej. WKŁ, Warszawa 2001
[3] Kamionka-Mikuła H., Małysiak H., Pochopień B., Układy cyfrowe. Teoria i przykłady. Wydawnictwo Pracowni Komputerowej Jacka Skalmierskiego. Wydanie III poszerzone. Gliwice 2001
[4] Majewski W., Układy logiczne. WNT, Warszawa 1993

SUBJECT SUPERVISOR

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