FACULTY OF ELECTRICAL ENGINEERING

SUBJECT CARD

Name in Polish:	**Projektowanie układów logicznych**
Name in English:	**Design of logic circuits**
Main field of study (if applicable):	**Electrical Engineering**
Specialization (if applicable):	**Control in Electrical Power Engineering**
Level and form of studies:	**2nd level, full-time**
Kind of subject:	**optional**
Subject code:	**ELR042136**
Group of courses:	**NO**

	Lecture	Classes	Laboratory	Project	Seminar
Number of hours of organized classes in University (ZZU):	15		15		
Number of hours of total student workload (CNPS):	60		30		
Form of crediting:	crediting with grade		crediting with grade		
For group of courses mark (X) final course:					
Number of ECTS points:	2		1		
including number of ECTS points for practical (P) classes :			1		
including number of ECTS points for direct teacher-student contact (BK) classes:	1.40		0.70		

PREREQUISITES RELATING TO KNOWLEDGE, SKILLS AND OTHER COMPETENCES

1. To be familiar with fundamentals of digital circuits.
2. To know how to practically interconnect simple digital circuits and verify their operation.
3. To be able to think and act in a creative way.
4. To be able to work in a team.

SUBJECT OBJECTIVES

C1. Gaining theoretical and practical knowledge on combinatorial logic circuits: canonical form, Karnaugh maps method, phenomenon of hazards.

C2. Gaining theoretical and practical knowledge on sequential logic circuits: the method of consecutive switching tables, Moore and Mealy type automata, races phenomenon.

C3. Familiarization with methods concerning: presenting a logic circuit operation, selecting of design methods, practical analysis/synthesis methods and ways of implementing logic circuits.

SUBJECT EDUCATIONAL EFFECTS

relating to knowledge:

PEK_W01 Has knowledge on operation, analysis and synthesis methods of combinatorial logic circuits.

PEK_W02 Has knowledge on operation, analysis and synthesis methods of sequential logic circuits.

relating to skills:

PEK_U01 Is able to conduct both analysis and synthesis, as well as to implement combinatorial logic circuits with use of the Karnaugh maps method, with eliminating a hazard phenomenon.

PEK_U02 Student is able to conduct both analysis and synthesis, as well as to implement asynchronous logic circuits with use of the method of consecutive switching tables, in particular Moore and Mealy types, with eliminating of races phenomenon.

PEK_U03 Student is able to conduct both analysis and synthesis, as well as to implement synchronous logic circuits.

relating to social competences:

PEK_K01 Student is able to act independently and cooperate within a group working on a complex engineering project.

PROGRAMME CONTENT		
Form of classes - lecture		**Number of hours:**
Lec 1	Introduction. Conditions for passing and marking the course. Basics of Boole algebra. Typical logic gates and circuits and their graphic symbols.	2
Lec 2	Design of combinatorial logic circuits.	2
Lec 3	Sequential automata – types, general characteristic, design principles.	2
Lec 4	Design of sequential automata with the method of consecutive switching tables.	2
Lec 5	Sequential automata – description of Moore and Mealy type automata.	2
Lec 6	Sequential automata – design steps.	2
Lec 7	Implementation of asynchronous sequential automata, elimination of races phenomenon and hazards.	2
Lec 8	Pass test.	1
	Total hours:	**15**

Form of classes - laboratory		**Number of hours:**
Lab 1	Presentation of health and safety rules, and general regulations of the laboratory. Conditions for passing and marking the course. General familiarization with the laboratory stands and simulative software.	2
Lab 2	Design of asynchronous sequential logic circuits with use of the transition tables and output maps. Implementation of circuits with use of logic gates - part 1.	2
Lab 3	Design of asynchronous sequential logic circuits with use of the transition tables and output maps. Implementation of circuits with use of logic gates - part 2.	2
Lab 4	Design of asynchronous sequential logic circuits with use of the transition tables and output maps. Implementation of circuits with use of flip-flops.	2
Lab 5	Design of asynchronous sequential logic circuits with the method of consecutive switching tables.	2
Lab 6	Multiplexers, de-multiplexers and code conversion circuits, adders, subtractors, comparators, counters and memory registers - investigation of selected circuit.	2
Lab 7	Design of synchronous sequential logic circuits.	2
Lab 8	Summary of laboratory excercises.	1
	Total hours:	**15**

TEACHING TOOLS USED
N1. Informative lecture.
N2. Didactic models of digital circuits.
N3. Programmme for simulating digital circuits.
N4. Report on performed laboratory excercise.
N5. Student's own work.

EVALUATION OF SUBJECT EDUCATIONAL EFFECTS ACHIEVEMENT		
Evaluation *F – forming (during semester)* *P – concluding (at semester end)*	**Educational effect number**	**Way of evaluating educational effect achievement**
F1(W)	PEK_W01 PEK_W02	Presence at the lectures
F2(W)	PEK_W01 PEK_W02	Crediting test
P(W)	P=0,1F1+0,9F2	
F1(L)	PEK_U01 PEK_U02 PEK_U03 PEK_K01	Activity at the laboratory
F2(L)	PEK_U01 PEK_U02 PEK_U03 PEK_K01	Reports from the laboratory assignements
P(L)	P=0,3F1+0,7F2	

PRIMARY AND SECONDARY LITERATURE

PRIMARY LITERATURE:

[1] Mano M. Morris, Digital design (second edition), Prentice-Hall Int., Inc., Englewood Cliffs, New Jersey, 1991.
[2] M. Morris Mano, C. R. Kime: Logic and computer design fundamentals, Pearson Prentice-hall Int., 2004, 3rd ed.
[3] Tocci R.J., Digital Systems. Principles and applications, Prentice-Hall Int., Inc., London, 1988.

SECONDARY LITERATURE:

[1] Układy logiczne. Ćwiczenia laboratoryjne. Skrypt Politechniki Wrocławskiej pod red. Mirosława Łukowicza. Oficyna Wydawnicza Politechniki Wrocławskiej, Wrocław, 2002
[2] Wilkinson B., Układy cyfrowe. WKŁ, Warszawa, 2000
[3] Skorupski A., Podstawy techniki cyfrowej. WKŁ, Warszawa, 2001
[4] Kamionka-Mikuła H., Małysiak H., Pochopień B., Układy cyfrowe. Teoria i przykłady. Wydawnictwo Pracowni Komputerowej Jacka Skalmierskiego. Wydanie III poszerzone. Gliwice 2001.

SUBJECT SUPERVISOR

Jan Iżykowski, jan.izykowski@pwr.edu.pl

MATRIX OF CORRELATION BETWEEN EDUCATIONAL EFFECTS FOR SUBJECT
ELR042136 - Design of logic circuits
AND EDUCATIONAL EFFECTS FOR MAIN FIELD OF STUDY **Electrical Engineering**
AND SPECIALIZATION **Control in Electrical Power Engineering**

Subject educational effect	Correlation between subject educational effect and educational effects defined for main field of study and specialization (if applicable)	Subject objectives	Programme content	Teaching tool number
PEK_W01	S2CPE_W16	C.1	Lec1 Lec2 Lec8	N.1 N.5
PEK_W02	S2CPE_W16	C.2	Lec1 Lec3 Lec4 Lec5 Lec6 Lec7 Lec8	N.1 N.5
PEK_U01	S2CPE_U15	C.3	Lab1 Lab2 Lab3 Lab4 Lab5 Lab6 Lab7	N.2 N.3 N.4 N.5
PEK_U02	S2CPE_U15	C.3	Lab1 Lab2 Lab3 Lab4 Lab5 Lab6 Lab7	N.2 N.3 N.4 N.5
PEK_U03	S2CPE_U15	C.3	Lab1 Lab2 Lab3 Lab4 Lab5 Lab6 Lab7	N.2 N.3 N.4 N.5
PEK_K01	K2ETK_K01 K2ETK_K02 K2ETK_K07	C.1 C.2 C.3	Lab1 Lab2 Lab3 Lab4 Lab5 Lab6 Lab7 Lab8	N.2 N.3 N.4 N.5